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SUPPLEMENTAL COPY OF APPLICATION

A New Method Of Digital FM Demodulator

BACKGROUND OF THE INVENTION

1. Field of the invention

Present invention relates to a new method of digital frequency-modulation demodulator and more particularly, to a digital frequency-modulation demodulator that using the structure of time-to-digital converter and the concept of delta-sigma analog-to-digital converter.

2. Prior Art

Frequency modulation (FM) is one of important and common method in communication system that its receiver end contains the FM detection circuit which often using analog design circuit and the final analog style FM demodulation circuit including detector circuit and lock loop circuit. If bring the detector into integrated circuit then it need chip area, and if implement PLL into integrated circuit then an external chip is necessary outside this chip.

Demodulated signal need the digital signal process after detection? then the above two circuit need analog-to-digital converter to convert the demodulated analog signal into digital signal. meanwhile, this digital signal is easy to be interfered by noise signal. However, the digital FM detector will first convert the modulation intermediate-frequency (IF) signal

int signal by way of analog-to-digital converter, then using digital signal
pr to demodulate this modulation signal. The analog-to-digital converter
ai signal processor used in digital FM demodulator must have fast
sp demodulate the modulation signal in real time. It also could use
re clock with multiple-fold frequency of modulation signal for sampling
t modulation signal to detect its phase change then demodulate, but
s this technology need a high frequency reference clock.
t conventional methods of digital RF communication system always need
t to convert the analog signal into digital signal in the receiver end with
c that increasing the circuit complexity. Thus, the demodulation circuit
c the detector circuit or PLL with analog-to-digital circuit could simply
t design also will be one of major objectives today.

SUMMARY OF THE INVENTION

before a primary objective of the present invention to provide a new
f digital FM demodulator will be applicable in radio communication
nsides, the modulation-demodulation section in receiver end also
pplicable in BB call, cellular phone, GPS system, and DECT system.

ext objective of the present invention is to provide a digital FM
tor with two function of modulation-demodulation and analog-to-digital

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to
The input intermediate-frequency signal pass through this invention
will generate a digital signal including high-frequency quantized
by way of a low-pass filter to filter out above quantized noise signal
baseband signal.

er objective of the present invention is to provide a digital FM
r which adopt the PLL structure and utilize the concept of delta-
og-to-digital converter which without connect external component
quency reference clock so that easy for integration.

vention with advantages that not only use delay lines as the timing
but also adopt the concept of delta-sigma analog-to-digital converter
the time-to-digital conversion for digital FM demodulator. This digital
ulator including delay lines, m-to-1 multiplexer, phase
arge pump circuit, quantizer and digital integrator. The modulation
intermediate frequency segment pass through the delay lines with the
around one cycle time and this delayed signal compare its phase
al signal. This compared pulse will go through charge pump circuit
nt into a voltage level stored in capacitor. This quantized voltage is
ed by the digital integrator, then sample another output signal of
; and compare phase with input signal. This system is similar to PLL,
ack system. The quantized digital signal will feed through low-pass

filter out high frequency noise and get the original modulation signal, the modulation signal is a digital signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit block diagram of digital FM demodulator according to the present invention, FIG. 2 is a circuit waveform of digital FM demodulator according to the present invention, and FIG. 3 is a system structure of digital FM demodulator according to the present invention.

FIG. 1 is a circuit block diagram of digital FM demodulator according to the present invention.

FIG. 2 is a circuit waveform of digital FM demodulator according to the present invention.

FIG. 3 is a system structure of digital FM demodulator according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Refer to Fig.1 that relates to the circuit block diagram of digital FM demodulator. The modulation signal $A_i(t)$ is fed into reference delay lines 111 and 112. The total delay time of delay lines 111 including coarse delay line 111 and fine delay line 112 is controlled separately by $A_i(t)$. The fine delay lines 112 has multiple output signals $A_{i1}(t), A_{i2}(t), \dots, A_{ij}(t)$ which could be expressed as follow:

$$A_{ij}(t) = A_i(t) \cdot e^{-j \cdot \frac{2\pi}{T} \cdot (c_j - d_j) \cdot t} \quad (1)$$

where c_j is fixed delay time of coarse delay lines and d_j is delay time of fine delay lines.

Phase detector compares the phase difference between A_{id} and A_i , then generate up and down signal. The m-to-1 multiplexer will select one of output signals $A_{i1}(t), A_{i2}(t), \dots, A_{ij}(t)$ from fine delay lines 112 and name it as A_{id} . If the rising edge of A_{id} signal lead the A_i signal, up signal will generate an effective pulse and its pulse width is just same as the time difference between the rising edges of A_i and A_{id} , but down signal do not generate any pulse. The total delay time of A_i signal pass through delay lines is T and the pulse width will equal to " $T - T_c - d \cdot T$ " when " $T_c + d \cdot T$ " smaller than T of A_i signal.

In the same way, if the rising edge of A_{id} signal lag the A_i signal, down signal will generate an effective pulse and its pulse width is also just same as the time difference between the rising edges of A_{id} and A_i signal, and the pulse width will equal to " $T_c + d \cdot T - T$ ".

positive when Aid lead the Ai signal, on the contrary, its value is negative when Aid lag Ai signal. Both effective pulse of up and down signal will charge pump circuit 14 for charging and discharging to capacitor Cc to generate a voltage difference, Vf, and its voltage level is proportional to difference or phase difference of Aid and Ai signal.

of input modulated signal will generate a Vf which is accumulated in capacitor Cc and this stored voltage will be quantized to generate a bit signal $y(k)$, $y(k)$ is the output digital sequence of total system.

15 is a analog-to-digital converter which could be one bit or converter. One bit converter is the comparator. The quantizer 15 in adopt one bit voltage comparator.

egrator 16 accumulate output digital signal $y(k)$, actually, it is simply counter due to quantizer 15 is one bit analog-digital converter. The output signal will select one output Aid signal from the fine delay lines multiplexer and compare its phase with Ai signal. Consequently, the Aid signal is controlled by output signal $y(k)$ it will delay one more $(k)=1$. On the contrary, the delay of Aid decrease one unit delay if $y(k)=0$, this whole system is similar to PLL structure. $Y(k)$ is feedback to aid delay time and make the next rising edge of Ai signal arrive detector with rising edge of Aid signal simultaneously, so the Aid signal lead one cycle than Ai signal when the system is locked.

In Fig.2, this is the circuit waveform of digital FM demodulator in the present invention. $T(k)$ is the k th cycle time of input modulation signal. $\Delta T(k)$ is the time difference of A_{id} rising edge with next A_i cycle. The up signal means $P(k)$ is positive value, but the down signal is negative. That is because the maximum frequency shift of input signal is much smaller than carrier frequency. The change of $T(k)$ is relative to carrier cycle T_c .

The effective pulse of up signal and down signal only happen at the rising edge of A_{id} and A_i signal and this effective pulse has been transferred to the capacitor C_c by way of charge pump circuit before arriving of $V_{(k-1)}$. This falling edge could be the trigger clock of the quantizer and

As this system do not need external reference clock. As shown in the diagram, a formula as follows :

$$T(k) = T(k-1) + y(k) * \tau \quad \text{--- (2)}$$

$$T(k-1) \quad \text{--- (3)}$$

we could get;

$$\Delta T(k) + y(k) * \tau \quad \text{--- (4)}$$

From the capacitor voltage at k th cycle based on Fig.2, we could calculate the signal is generated by $V(k-1)$ and I_c signal to charge/discharge C_c .

dur
own signal effective pulse period and I_b charge/discharge C_c
du, i.e. the voltage is determined by these three parameters.

Th
Cc for I_c at kth cycle is :

$$\Delta V = V(k) - V(k-1) \quad (5)$$

clock is the input modulation signal A_i , then the C_c voltage level
will be constant when charge-discharge is at kth cycle.

$$\Delta V = C_c * [T(k) + T(k+1)] / 2 \quad (6)$$

T:

$$\Delta V = V_f_b - V_f_a \quad (7)$$

$$V_f_b = y(k) * (I_b / C_c) * [T(k) + T(k+1)] / 2 + \{I_c / C_c * P(k)\} \quad (8)$$

maximum frequency shift is much smaller than carrier
 $T(k)$ is around equal to carrier cycle T_c

$$V_f_b = y(k) * (I_b / C_c * P(k) + I_c / C_c * P(k+1)) * T_c \quad (9)$$

A:

B:

C:

D:

E:

F:

G:

H:

I:

J:

K:

L:

M:

N:

O:

P:

Q:

R:

S:

T:

U:

V:

W:

X:

Y:

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$$V(k) = [P(k) + \Delta T(k) + y(k)^* T] + B^* y(k)$$

The output of $V(k)$ is the total system output.

In Fig.3, is the system structure of digital FM demodulator in the present invention. This diagram is a two level delta-sigma modulator. The input is $\Delta T(k)$ that also is the signal difference of $T(k)$ and $T(k-1)$. The output of the output signal $y(k)$ in present invention is similar to the analog-digital converter output signal. the quantized noise signal is a high frequency segment. So, the output digital signal $y(k)$ is filtered first then filter out quantized noise by the digital filter to get the final signal.

This technology is similar to conventional delta-sigma analog-to-digital converter. Based on above deduction, the output digital signal is the filtered version of original modulation signal. In brief, $y(k)$ signal filter out the noise by way of low-pass digital filter before signal accumulation.

This invention provide a FM digital demodulator which with more advantages than conventional technology as follow:

1. **b**rid circuit in present invention will be applicable in radio system, besides, the modulation-demodulation section in also could be applicable in BB call, cellular phone, GPS system, system.
2. **b**vention to provide a digital modulation demodulator which L structure and utilize the concept of delta-sigma analog-to-ter which without connect external component and high reference clock so that easy for integration.
3. **b**vention to provide a digital modulation demodulator with two demodulation and analog-to-digital conversion. The input of -frequency signal pass through this invention demodulator will digital signal including high-frequency quantized signal. then by pass filter to filter out above quantized noise signal to get the signal.

es and modifications in the above described embodiment of the in, of course, be carried out without departing from the scope of the invention, to promote the progress in science and the useful arts, the enclosed and is intended to be limited only by the scope of the a.